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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:	Examiner: K. Coulter
U.S. Patent No. 5,809,306	Group Art Unit: 2784
Masato Suzuki et al.	
Serial No.: 09/662,484	September 19, 2002
Reissue Filed: September 14, 2000	Irvine, California 92614
For: VARIABLE ADDRESS LENGTH COMPILER AND PROCESSOR IMPROVED IN ADDRESS MANAGEMENT	

SUPPLEMENTAL PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified Reissue application and in furtherance to the Preliminary Amendment filed on August 29, 2001, please enter the following amendments:

IN THE CLAIMS:

Please add the following new Claims:

80. (New) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit for holding data;

a second register unit for holding data;

a sign-extending unit for sign-extending data; and

a zero-extending unit for zero-extending data,

wherein said zero-extending unit zero-extends data when the instruction designates said first register unit and said sign-extending unit sign-extends said data when the instruction designates said second register unit.

81. (New) The processor of Claim 80, wherein the instruction includes a destination operand which designates one of said first register unit and said second register unit.

82. (New) The processor of Claim 81, wherein said data is an immediate data included in the instruction.

83. (New) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit for holding data;

a second register unit for holding data;

a sign-extending unit for sign-extending data;

a zero-extending unit for zero-extending data; and

an instruction decoding unit for decoding an instruction in the program to detect a first type instruction and a second type instruction, said first type instruction including an instruction to store data into said first register unit, said second type instruction including an instruction to store data into said second register unit, with said first type instruction and said second type instruction having different destination operands to designate whether to store data into said first register unit or said second register unit,

wherein said zero-extending unit zero-extends data when a first type instruction is detected and said sign-extending unit sign-extends said data when a second type instruction is detected.

84. (New) The processor of Claim 83, wherein said data is an immediate data included in the first type instruction and the second type instruction.

85. (New) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising the steps of:

decoding the instruction for selecting one of the first register and the second register in accordance with an operand of the decoded instruction;

zero-extending data when said decoded instruction designates the first register; and

sign-extending said data when said decoded instruction designates the second register.

86. (New) The data processing method of Claim 85, wherein the operand is a destination operand which designates one of the first register and the second register.

87. (New) The data processing method of Claim 86, wherein said data is an immediate data included in the instruction.